UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/503,140	02/11/2000	Tsuneo Hayashi	SONY-T0130	6142

33448 7590 05/26/2005

ROBERT J. DEPKE
LEWIS T. STEADMAN
TREXLER, BUSHNELL, GLANGLORGI, BLACKSTONE & MARR
105 WEST ADAMS STREET, SUITE 3600
CHICAGO, IL 60603-6299

EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/503,140	HAYASHI ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7,19,20 and 28-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,19,20 and 28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-3, 5-7, 19, 20 and 28-33 have been considered but are moot in view of the new ground(s) of rejection.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 28, 30 and 32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 28, 30 and 32 substantially recite "wherein the error correcting means employs a block number control circuit that charges a cumulative number of blocks based on a cumulative block number charge signal". Nowhere in the application does the Applicant even use the word charge nor does the Applicant teach the use of a charge signal.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 28, 30 and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 28, 30 and 32 substantially recite "wherein the error correcting means employs a block number control circuit that charges a cumulative number of blocks based on a cumulative block number charge signal", which is incomprehensible. In particular, it is not clear what is meant by charging "a cumulative number of blocks".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 19, 20 and 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi, Yasuhiro et al. (US 5784356 A, hereafter referred to as

Hayashi) in view of Bullock; Dean C. et al. (US 5764651 A, hereafter referred to as Bullock).

35 U.S.C. 103(a) rejection of claims 1 and 28.

Hayashi teaches a readout controlling apparatus for controlling reading conditions while reading data from a recording medium (See Abstract, System Controller 29 in Figure 7 and col. 4, lines 61-67 in Hayashi), comprising: an error correcting means for correcting errors in said read data (Correction Circuit 16 in Figure 7 of Hayashi is an error correcting means for correcting errors in said read data); an error rate calculating means for calculating an error rate of said errors in said read data (Error Rate Counter 31 is an error rate calculating means for calculating an error rate of said errors in said read data); and a control means for dynamically controlling and adjusting an amplitude of the signal superimposed on the signal applied to the laser diode (Figure 7 and col. 4, lines 61-67 in Hayashi teach the system controller 29 performs control to increase the gain of the variable gain amplifier 30 through the I/F circuit 26, thus increasing the amplitude of the RF signal; Note: pickup 12 superimposes the digital write signal onto a laser beam for transmission), based on the calculated error rate in order to reduce the error rate wherein the adjustment occurs while reading user data from the disc in response to the bit error rate exceeding a predetermined level (see Abstract in Hayashi: Note: the apparatus in Hayashi is designed to allow counter-measures against data read errors, hence is a means for dynamically controlling and adjusting an amplitude).

Note: in the phrase "an amount of light from a laser diode used in reading said data, or a frequency of a signal superimposed on a signal applied to the laser diode or an amplitude of the signal superimposed on the signal applied to the laser diode" only one of the statements connected by or logic is required to be true in order for the statement to be true, hence the previously quoted statement is true since the control means 29 in Figure 7 of Hayashi is for dynamically controlling and adjusting an amplitude of the signal superimposed on the signal applied to the laser diode (Figure 7 and col. 4, lines 61-67 in Hayashi teach the system controller 29 performs control to increase the gain of the variable gain amplifier 30 through the I/F circuit 26, thus increasing the amplitude of the RF signal; Note: pickup 12 superimposes the digital write signal onto a laser beam for transmission).

However Hayashi does not explicitly teach the specific use of an error correcting means comprised of a plurality of counters and registers with at least one reset signal generator.

Bullock, in an analogous art, teaches use of an error correcting means comprised of a plurality of counters (WIN LEN and DEN COUNT in steps 38, 44 and 46 in Figure 7 of Bullock ARE CONTERS) and registers (see registers in Figure 6 of Bullock) with at least one reset signal generator (Step 54 in Figure 7 of Bullock is a reset signal generator). Note: Figure 7 of Bullock is a typical BER calculating scheme.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayashi with the teachings of Bullock by including use of an error correcting means comprised of a plurality of counters and registers with at least

one reset signal generator. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an error correcting means comprised of a plurality of counters and registers with at least one reset signal generator would have provided a means for calculating the required error rate in the Hayashi patent.

35 U.S.C. 103(a) rejection of claims 19 and 30.

Hayashi teaches a recorder for recording data on a storage medium (See Abstract, System Controller 29 in Figure 7 and col. 4, lines 61-67 in Hayashi), comprising: a reading means for reading recorded data (see Pickup 12 in Hayashi); an error correcting means for correcting errors in data read by the reading means (Correction Circuit 16 in Figure 7 of Hayashi is an error correcting means for correcting errors in said read data); an error rate calculating means for calculating an error rate (Error Rate Counter 31 is an error rate calculating means for calculating an error rate of said errors in said read data); and a control means for dynamically controlling and adjusting one or more of the following recording characteristics (Figure 7 and col. 4, lines 61-67 in Hayashi teach the system controller 29 performs control to increase the gain of the variable gain amplifier 30 through the I/F circuit 26, thus increasing the amplitude of the RF signal): a frequency of a signal superimposed on a signal applied to the laser diode; or a speed of said recording medium wherein the adjustment occurs while reading user data from the disc in response to the bit error rate exceeding a predetermined value (Step 134 of Figure 125 in Hayashi is a means for dynamically controlling and adjusting

the speed of said recording medium wherein the adjustment occurs while reading user data from the disc in response to the bit error rate exceeding a predetermined value, Note: only one of the statements connected by or logic is required to be true in order for the statement to be true).

However Hayashi does not explicitly teach the specific use of an error correcting means comprised of a plurality of counters and registers with at least one reset signal generator.

Bullock, in an analogous art, teaches use of an error correcting means comprised of a plurality of counters (WIN LEN and DEN COUNT in steps 38, 44 and 46 in Figure 7 of Bullock ARE CONTERS) and registers (see registers in Figure 6 of Bullock) with at least one reset signal generator (Step 54 in Figure 7 of Bullock is a reset signal generator). Note: Figure 7 of Bullock is a typical BER calculating scheme.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayashi with the teachings of Bullock by including use of an error correcting means comprised of a plurality of counters and registers with at least one reset signal generator. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an error correcting means comprised of a plurality of counters and registers with at least one reset signal generator would have provided a means for calculating the required error rate in the Hayashi patent.

35 U.S.C. 103(a) rejection of claims 20 and 32.

Hayashi teaches a readout controlling apparatus for controlling reading conditions while reading data from a recording medium (See Abstract, System Controller 29 in Figure 7 and col. 4, lines 61-67 in Hayashi), comprising: an error correcting means for correcting errors in said read data (Correction Circuit 16 in Figure 7 of Hayashi is an error correcting means for correcting errors in said read data); an error rate calculating means for calculating an error rate of said errors in said read data (Error Rate Counter 31 is an error rate calculating means for calculating an error rate of said errors in said read data); and a control means for dynamically controlling and adjusting an amplitude of the signal superimposed on the signal applied to the laser diode (Figure 7 and col. 4, lines 61-67 in Hayashi teach the system controller 29 performs control to increase the gain of the variable gain amplifier 30 through the I/F circuit 26, thus increasing the amplitude of the RF signal; Note: pickup 12 superimposes the digital write signal onto a laser beam for transmission), based on the calculated error rate in order to reduce the error rate wherein the adjustment occurs while reading user data from the disc in response to the bit error rate exceeding a predetermined level (see Abstract in Hayashi: Note: the apparatus in Hayashi is designed to allow counter-measures against data read errors, hence is a means for dynamically controlling and adjusting an amplitude). Note: in the phrase "an amount of light from a laser diode used in reading said data, or a frequency of a signal superimposed on a signal applied to the laser diode or an amplitude of the signal superimposed on the signal applied to the laser diode" only one of the statements connected by or logic is required to be true in order for the statement to be true, hence the previously quoted statement is true since the control means 29 in

Figure 7 of Hayashi is for dynamically controlling and adjusting an amplitude of the signal superimposed on the signal applied to the laser diode (Figure 7 and col. 4, lines 61-67 in Hayashi teach the system controller 29 performs control to increase the gain of the variable gain amplifier 30 through the I/F circuit 26, thus increasing the amplitude of the RF signal; Note: pickup 12 superimposes the digital write signal onto a laser beam for transmission).

Note: The Abstract of Hayashi teaches that amplitude is adjusted by adjusting the gain. In addition, the claim language of claim 20 is a subset of the claim language in claim 1 except for the use of the term "gain".

However Hayashi does not explicitly teach the specific use of an error correcting means comprised of a plurality of counters and registers with at least one reset signal generator.

Bullock, in an analogous art, teaches use of an error correcting means comprised of a plurality of counters (WIN LEN and DEN COUNT in steps 38, 44 and 46 in Figure 7 of Bullock ARE CONTERS) and registers (see registers in Figure 6 of Bullock) with at least one reset signal generator (Step 54 in Figure 7 of Bullock is a reset signal generator). Note: Figure 7 of Bullock is a typical BER calculating scheme.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayashi with the teachings of Bullock by including use of an error correcting means comprised of a plurality of counters and registers with at least one reset signal generator. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill

in the art would have recognized that use of an error correcting means comprised of a plurality of counters and registers with at least one reset signal generator would have provided a means for calculating the required error rate in the Hayashi patent.

35 U.S.C. 103(a) rejection of claims 29, 31 and 33.

Figure 7 and col. 4, lines 61-67 in Hayashi teach the system controller 29 performs control to increase the gain of the variable gain amplifier 30 through the I/F circuit 26, thus increasing the amplitude of the RF signal; Note: pickup 12 superimposes the digital write signal onto a laser beam for transmission. The system controller 29 is substantially a selection means for selecting and controlling the gain.

4. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi, Yasuhiro et al. (US 5784356 A, hereafter referred to as Hayashi) and Bullock; Dean C. et al. (US 5764651 A, hereafter referred to as Bullock) in view of Takamine, Kouichi et al. (US 6240055 B1, hereafter referred to as Takamine).

35 U.S.C. 103(a) rejection of claims 2 and 3.

Hayashi and Bullock, substantially teaches the claimed invention described in claim 1 (as rejected above). In addition, Hayashi teaches said data is coded in units of code blocks (in col. 4, lines 33-46, Hayashi teaches the use of a C1xC2 product code); and said error correcting means corrects errors in said code blocks (in col. 4, lines 33-46, Hayashi teaches C1 correction processing). The Examiner would like to point out that

generally product code error correcting techniques not only have the ability to correct errors but to also detect uncorrectable errors and that error rate consists of correctable as well as uncorrectable errors, i.e., all detectable errors.

However Hayashi and Bullock, does not explicitly teach the specific use of a specific error correction technique that is capable of detecting uncorrectable errors to be added to the correctable errors in determining the bit rate.

Takamine, in an analogous art, teaches the use of CRC which is an error correcting techniques with the ability to correct errors but to also detect uncorrectable errors (col. 25, lines 63-67, Takamine). The Examiner would like to point out that error rate consists of correctable as well as uncorrectable errors, i.e., all detectable errors.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayashi and Bullock with the teachings of Takamine by including the specific use of an error correction technique that is capable of detecting uncorrectable errors to be added to the correctable errors in determining the bit rate. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that an error correction technique that is capable of detecting uncorrectable errors to be added to the correctable errors in determining the bit rate would provide the opportunity to calculate the total detectable error rate (Note: error Rate is a standard calculation based on detectable errors).

5. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi, Yasuhiro et al. (US 5784356 A, hereafter referred to as Hayashi), Bullock; Dean C. et al. (US 5764651 A, hereafter referred to as Bullock) and Takamine, Kouichi et al. (US 6240055 B1, hereafter referred to as Takamine) in view of in view of Lee, Woo-Nyun et al. (US 5930448 A, hereafter referred to as Lee).

35 U.S.C. 103(a) rejection of claim 5.

Hayashi, Bullock and Takamine, substantially teach the claimed invention described in claims 1-3 (as rejected, above). In addition, Hayashi teaches said data is coded in units of code blocks (in col. 4, lines 33-46, Hayashi teaches the use of a C1xC2 product code); and said error correcting means corrects errors in said code blocks (in col. 4, lines 33-46, Hayashi teaches C1 correction processing). The Examiner would like to point out that product codes are a general error-correcting technique primarily used for recording mediums using inner and outer codes arranged in columns and rows. However, Hayashi, Bullock and Takamine, do not explicitly teach the specific use of Inner and outer code **arranged in columns and rows**.

Lee, in an analogous art, teaches the specific use of Inner and outer code **arranged in columns and rows** (See Figure 1, Lee).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayashi, Bullock and Takamine with the teachings of Lee by including use of Inner and outer codes **arranged in columns and rows**. This modification would have been obvious to one of ordinary skill in the art, at the time the

invention was made, because one of ordinary skill in the art would have recognized that use of readily available error correcting techniques such as Inner and outer codes **arranged in columns and rows** would provide the opportunity to calculate a bit error rate (see Fig. 3, Lee).

35 U.S.C. 103(a) rejection of claim 6.

See RAM 17 in Figure 7, Hayashi.

35 U.S.C. 103(a) rejection of claim 7.

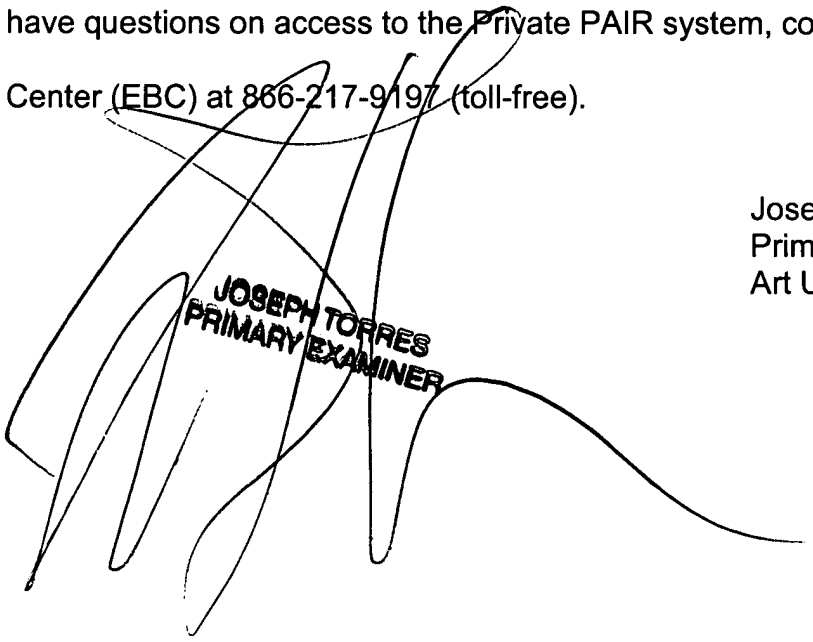
Col. 15, lines 9-14 in Takamine teach that parity errors are counted for use in calculating error rates; hence the error rate is based on cumulative addition values.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133